FEW ELECTRON QUANTUM DOTS
IN InAs/InP CORE SHELL NANOWIRES

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Chapter 1

Introduction

“To boldly compute what no man has computed before . . . ”

Much effort is being directed at harnessing the potential power of quantum computing [7]. At the turn of the millennium Loss and DiVincenzo proposed to use the quantum mechanical spin states of an electron, confined in a single electron semiconductor quantum dot to encode quantum information [6]. With current state of the art lithography technology it is possible to fabricate quantum dots using semiconductors at nanometer scales. Isolation of single electrons, preparing and manipulating spin states has been demonstrated with great success [14, 12, 23, 22]. Interaction of the electron spin with the environment leads to decoherence and thus loss of quantum information. Electrons in quantum dots in GaAs/AlGaAs heterostructures suffer decoherence due to hyperfine interaction with the nuclear spins of the surrounding atoms in $\sim 10$ ns [23]. This poses limits on time to implement the quantum algorithm and read out the qubits. InAs is of particular interest amongst the III-V materials, with a small bandgap ($E_g=0.35$eV), compared to GaAs ($E_g=1.4$eV) and thus a strong spin-orbit interaction. Bulk InAs has a $g$-factor of -14.7 whereas for bulk GaAs it is -0.44. With a smaller effective mass ($m^*=0.023m_0$ for InAs and 0.067$m_0$ for GaAs) and smaller spin orbit length ($l_{SO} \sim 130$ nm for InAs [11] and $\sim 1 \mu$m for GaAs), coherent manipulation of the electron spin using an oscillating electric field (EDSR) is expected to be orders of magnitudes faster. To this effect, InAs nanowires with a thin shell of InP, are explored as a system where a quantum dot can be defined and probed electrically. InAs has the Fermi level pinning in the conduction band at the surface.
Ohmic contacts can thus easily be fabricated to the nanowire. Nanowires offer a bottom up approach to exploring 1 D systems. Semiconductor crystalline nanowires of high purity can be grown with control over the radial and axial dimensions. The possibility of growing radial and axial heterojunctions with defect free interfaces, and control of chemical composition and structure, nanowires are excellent candidates for building blocks for such research directions.

It would be interesting to study the effect of electron confinement on its g-factor. The effective g-factor of an electron depends on the ground state energy, the relative proportion of the wave function in different materials for heterostructures, and the valence band mixing. In a quantum dot, by moderating gate voltages one can affect the shape and size of the dot, energy levels and thus $g^*$. In a series of quantum dots along a nanowire, this can be used to bring an electron spin in a specific quantum dot in and out of resonance with an oscillating field (ESR) [9].

1.1 Acknowledgements

I would like to thank the Erasmus Mundus program for giving me the opportunity to study in two different universities and countries. I have learnt much from the exposure to the different academic environments. I have seen and experienced cultures of two different countries. I am grateful to Leo for giving me the opportunity to work at QT. I have never before seen a place so alive with activity. I am obliged to Katja, for if it weren’t for her I wouldn’t have heard about nanowires. Juriaan, my daily supervisor has been both a mentor and a friend through the project. I have enjoyed all our discussions in the course of the year, be it about flipping electrons or the economical prospects of male escorts to rich old spinsters in the Netherlands. I am also grateful to Sergey, Gary and Stevan for discussions about quantum dots. I am amazed at how seemingly complex things can be deconstructed and explained in a simple manner. I am grateful to Diana, for being there.
Chapter 2

Theory

A quantum dot is a region with confinement of electrons (or holes) in the 3 spatial directions. The addition of an electron to a quantum dot costs energy which leads to a Coulomb blockade, if the energy cannot be supplied. If this is the case, the number of electrons on the dot remain constant. Spatial confinement leads to quantization of energy within the dot. Current lithographic techniques allows for the fabrication of nanometer scale structures. This coupled with the low effective mass in semiconductors (0.023 $m_0$ in InAs, 0.067 $m_0$ in GaAs) allows single particle levels with spacing comparable to the charging energy. Addition of electrons to a quantum dot generally obeys Hund’s rule for shell filling [24], and tunnel coupling between two dots can be compared to molecular bonding. Depending on the strength of the interdot coupling, two dots can form ioniclike (weak tunnel coupling) to covalentlike bonds (strong tunnel coupling) [29]. The symmetry of a quantum dot in a two dimensional cylindrically symmetric harmonic potential leads to a two-dimensional shell structure with magic numbers 2, 6, 12, 20... [19] Quantum dots have been compared to artificial atoms [19, 18, 4]. A quantum dot can be electrically coupled to electron/hole reservoirs via tunnel barriers allowing current to run. Electrostatistically coupled gates can be used to shift the electrochemical potential level of the dot, thus changing the number of electrons trapped on such a island. A semiconductor quantum dot is thus, a tunable structure for trapping and manipulating single charges.
2.1 The constant interaction model

The electronic properties and transport through a quantum dot can be understood through the constant interaction model [19, 22, 20]. The model makes two assumptions:

- Coulomb interaction of the electrons in the dot with the environment (gate, the source and the drain) can be expressed through capacitances (Fig. 2.1). The total capacitance of the dot $C$, is a sum of the capacitances between the dot and the gate $C_G$, the source $C_S$ and the drain $C_D$. All gates that couple to the dot contribute to the total capacitance, $C = C_S + C_D + C_G$.

- The energy level separation is independent of the number of electrons and the interaction between the latter.

![Figure 2.1: Equivalent circuit of the quantum dot for the constant interaction model](image)

To add an electron to a dot, a certain amount of energy is needed to overcome the electrostatic repulsion due to other electrons. This is termed as charging energy, $E_C$. As a result of quantization of the energy due to confinement, additional energy is needed determined by the spacing $\Delta E$ between two quantum levels. This can be zero if two consecutive electrons are added to the same spin-degenerate level. The total energy of the dot as a function of the number of electrons in the dot, $U(N)$ can thus be calculated:

$$U(N) = \left[ -|e|(N - N_0) + C_S V_S + C_D V_D + C_G V_G \right]^2 + \sum_{n=1}^{N} E_n(B)$$ (2.1)

$e$ is the electron charge, $N_0$ is the background charge due to pre-existing charges and donors, B is the magnetic field and $E_n$ corresponds to the eigenenergies of the
dot in the presence of a magnetic field and a confining potential. The electrochemical potential is defined as:

$$\mu(N) = U(N) - U(N-1) = (N - N_0 - \frac{1}{2})E_C - \frac{E_C}{|e|}(C_SV_S + C_DV_D + C_GV_G) + E_n$$  \hspace{1cm} (2.2)$$

$$E_C = e^2/C$$ is the charging energy. The electrochemical potential, i.e., the difference in the ground state energies of the dot with \(N\) and \(N-1\) electrons, represents the amount of energy needed to add an extra electron to a system with \(N-1\) electrons. The energy needed to add the next electron is higher by an amount:

$$E_{add}(N) = \mu(N + 1) - \mu(n) = E_C + \Delta E$$ \hspace{1cm} (2.3)$$

\(E_C\) is the pure electrostatic part, and \(\Delta E\) is the level spacing between two consecutive energy levels within the dot. For an electron added to the same shell, \(E_{add}\) is simply the charging energy, \(E_C\). For the same electron added to the next shell, it comprises an additional amount, the orbital energy or level spacing, \(\Delta E\).

Whereas the energy of the dot is dependent on the square of the gate potential, the electrochemical potential has a linear dependence for all \(N\). Electrochemical potential levels can be looked upon as a ladder which can be shifted up and down by tuning \(V_G\) (Equ. 2.2), while the distance between the levels remains constant (Fig. 2.2(a)).

The difference between the Fermi levels in the source and drain reservoirs is referred to as the bias window, \(\mu_s - \mu_d = -|e|V_{SD}\). Referring to the Fig. 2.2, electron transport through the dot occurs if there lies an energy level within this bias window, else the dot remains Coulomb blockaded. Sweeping the gate voltage shifts this ladder across the bias window leading to coulomb oscillations.

A tunnel barrier is characterized by a resistance. The Heisenberg’s uncertainty relation, \(\Delta E \Delta t \geq \hbar/2\) poses conditions on the tunnel barriers forming the dot. \(\Delta E\) is the uncertainty or the spread in the energy level of the dot, and \(\Delta t\) is the electron residence time on the dot (charging or discharging time of the dot). Rearranging terms in the uncertainty relation, with \(E_C\) as the charging energy, one gets \(\Delta E \sim \frac{E_C}{R/|h/e^2|}\). If the barrier resistance \(R\) is of the order \(\hbar/e^2\), the uncertainty in the energy level is of the order of the charging energy. If the levels in the dot overlap, the electron state within the dot is not be well defined. Another limitation is posed by temperature.
Electrons should not be able to overcome the Coulomb blockade due to thermal activation, i.e, $E_C > k_b T$.

Typically, the measurements are carried out by grounding the drain and varying the voltage applied to the source and gates. Depending on the size of the bias window, transport through the dot can be understood in two regimes - the low bias regime and the high bias regime.

![Figure 2.2](image)

**Figure 2.2:** Electrochemical potential levels in the two regimes (a) The schematic depiction of the electrochemical potential ladder in the low bias regime. Transport occurs when an energy level lines up with the source-drain, and is marked by a peak in current. The dot remains in Coulomb blockade and the number of electrons on the dot is constant otherwise. The spacing between the current peaks indicates the addition energy. (b) The electrochemical potential levels in the high bias regime. Two scenarios depicted here correspond to when level spacing is larger and smaller than the bias window respectively.

### 2.1.1 Low bias regime

The low bias regime is characterized by $-|e|V_{sd} < \Delta E, E_{add}$. Only one level can lie within the bias window since $\mu_S - \mu_D \approx 0$. Transport occurs only through the ground state. On varying $V_G$, the Coulomb blockade is lifted when a level comes within the bias window and electrons can tunnel and go through the dot, one at a time. This is
referred to as single electron tunneling. The periodic oscillation or peaks versus $V_G$ indicate the lifting of the blockade, as electrons pass through the dot (Fig. 2.2(a)). The shape of the peak depends on the temperature and tunneling rate of electrons through the dot. The height of the peak depends on the tunnel coupling of the level with lead [30, 19]. The spacing between the peaks is a measure of the addition energy.

### 2.1.2 High bias regime

The high bias regime is characterized by $-|e|V_{sd} > \Delta E$ and/or $-|e|V_{sd} > E_{add}$. Multiple electrochemical potential levels may lie within this window. Starting with the low bias regime, as $V_{SD}$ is increased eventually a level corresponding to a transition through an excited state falls within the window. There will be two paths available for an electron to tunnel through the dot. This is still single electron tunneling. As $V_{SD}$ is increased further, the bias window can become larger than charging energy $E_C$, and transitions involving the next ground state become possible Fig. 2.3(a). The contribution of these states to the current depends on their respective tunnel couplings. The tunnel coupling $\Gamma$, depends on the overlap between the wave function of the dot and the leads. The size of the bias window gives the addition energy directly as, $E_{add} = eV_{SD}$ (Fig. 2.3(b)).

### 2.1.3 Coulomb Diamonds

Stability diagram of a quantum dot is obtained by plotting the current $I$ or differential conductance $dI/dV_{SD}$ as a function of the bias $V_{SD}$ and gate voltage $V_G$.

In order to calculate and plot the differential conductance as a function of bias and gate voltage (Fig. 2.3(a)), eqn. 2.2 can be used to calculate the relevant ground and excited state energies. These are summarized as:

$$U_{ES}(N) = U_{GS}(N) + \Delta E(N)$$
$$U_{GS}(N + 1) = U_{GS}(N) + E_{add}$$
$$\mu_{a\rightarrow b} = U_b(N) - U_a(N - 1)$$

$U_{GS}$ and $U_{ES}$ are the energies of the dot in the ground and excited state respectively. As $V_G$ is changed, different levels align either with the source or the drain.
Figure 2.3: (a) Possible transitions at high bias, the corresponding electrochemical potential ladder and a schematic plot of differential conductance as a function of $V_{SD}$ and $V_G$.[22]. (b) Schematic of a Coulomb diamond. The black lines correspond to transition through ground states of the dot, and the red correspond to the excited state transitions. Various parameters such as the addition energy, orbital energy and the $\alpha$ factor can be extracted as shown from the diamond.

Current flows and this is marked by a step in the conductivity. The lines shown in Fig. 2.3 mark such a situation. The transition through excited states terminate on the edges of the diamond. As a rule of thumb, a line that terminates on an N-electron diamond involves an N-electron excited state [22]. Coulomb blockade occurs inside the diamond shaped regions. The number of electrons in the dot remains constant within a diamond. As indicated in the Fig 2.3(b), the height of a diamond is a measure of addition energy, $E_{add}$. The width of a diamond, $\Delta V_G$ can be related to energy as: $\alpha \Delta V_G$. $\alpha$ is the lever arm factor of the gate, being the ratio of the gate capacitance to the dot to the total capacitance. It relates a change in gate voltage to a change in energy. As the dot size shrinks with decreasing electron number N, the dot capacitance C, increases. $\alpha$ thus changes with $V_G$. As electrons are added to an empty quantum dot, the increase in dot size is evident from the decreasing trend in the addition energy $E_{add}$. The charging energy $E_C$, and orbital energy, $\Delta E$, scale inversely with the size of the dot. Thus at low N (small dot) there is a large variation in $E_{add}$, and at higher N (large dot) the variation is small (Fig. ??). The diamond corresponding to the empty dot does not close for a large bias and no lines corresponding to transitions through excited states end on the $N = 0$ diamond edge. Any line
Figure 2.4: (a) The figure shows Coulomb diamonds as electrons are added to the dot. Variation in $E_{add}$ is visible from the size of the diamonds. (b) Coulomb peaks. Inset: Variation of $E_{add}$ with N at zero magnetic field. Figures from [19]

ending on this would imply a transition involving n=0 electrons. However, energy absorption from the environment can lead to phonon or photon assisted tunneling giving rise transition lines ending on this diamond edge.

There are a few distinct aspects of the charge stability diagram evident when N is low ($\lesssim 20$). The eigen energies $E_{n,l}$, as a function of B can be solved analytically for a two dimensional harmonic confinement characterized by $V(r) = 1/2m^*\omega r^2$. This spectrum is depicted in Fig. 2.5(b). In the absence of a magnetic field the eigenenergies of the dot are given by $E_{n,l} = (2n + |l| + 1)\hbar\omega_0$. n=0,1,2,... is the radial quantum number, $l = 0, \pm 1, \pm 2...$ is the angular momentum quantum number and $\omega_0$ is the oscillator frequency, characteristic of the confining potential. The first shell
Figure 2.5: (a) Variation of addition energy with electron number N at different magnetic fields B. The orbital degeneracy is lifted with magnetic field reflected in the variation of $E_{\text{add}}$ which becomes smaller, and the curves smoother. The curves have been offset for clarity. The curves are plotted without any offset to highlight the decreasing trend with increasing N. (b) The calculated energy states in a dot versus the magnetic field, known as the Fock-Darwin spectrum for a parabolic potential with $\hbar \omega_0 = 3\text{meV}$. Figure from [19]

corresponds to n,l = 0,0 and can accommodate 2 electrons. The next shell has a double orbital degeneracy with $E_{0,1}=E_{0,-1}$ and can hold 4 electrons. The third shell has a triple orbital degeneracy with $E_{1,0}=E_{0,-2}=E_{0,2}$. This degeneracy however is specific for the 2D isotropic parabolic confinement [19, 26]. Shell filling can be observed as variation in the addition energy $E_{\text{add}}$ (or peak spacing) (Fig. 2.5(a)) with N. For N = 2, 6 and 12 a jump in $E_{\text{add}}$ is observed. Applying a magnetic field lifts the orbital and spin degeneracy. It should be mentioned that quantum dots presented later in the thesis do not have symmetric confining potentials. Due to this a trend of shell filling with magic numbers 2, 6, 12... due to degenerate shells is not observed. However, alternating size of the diamonds as electrons are added to an empty dot is observed.
2.1.4 Co-tunneling

Figure 2.6: Schematic depiction of co-tunneling and contributions to current within a Coulomb diamond. (b) and (e) depicts the situation when the level corresponding to transfer of electrons through an excited state is in resonance with the source and drain respectively. (c) and (d) depict elastic and inelastic co-tunneling events. Figure from [8].

As resistance of the tunnel barrier approaches $\hbar/e^2$, higher order tunneling events can become important [8, 17]. At low bias, transitions between well defined charge states within the dot is only possible if the energy supplied is greater than the charging energy. In the Coulomb blockade, two electrons can co-operate and current can flow without paying the charging energy. Such a process involves the tunneling of an electron into the dot, and another tunneling out of the dot. An electron tunneling into the dot may the electron may stay in the island during Heisenberg uncertainty time $t \approx \hbar E_C$. During the Heisenberg time, another electron may tunnel out of the dot through the other tunnel barrier. It is a second order process with the tunneling rate, $\Gamma_{CO} \propto \Gamma_L \Gamma_R$ where $\Gamma_L$ and $\Gamma_R$ are the tunneling rates for the left and right barrier. The charge on the dot does not change, but an electron is transferred from one side to another. At low bias, one electron can tunnel into a dot, while an electron
from the ground state tunnels out. This is known an elastic co-tunneling, and the dot remains in the ground state. When the bias is larger than level spacing, then an electron can tunnel into the excited state, while simultaneously an electron tunnels out from the ground state. This is known as inelastic co-tunneling, although the total energy is conserved. These processes are depicted in Fig. 2.6.

2.2 Diagonals

The gates defining the tunnel barriers also couple to the dot electrostatically. Sweeping one such gate, say to more negative voltages, has two effects. The tunnel coupling changes leading to a change in current. Due to the electrostatic coupling to the dot, it also raises the electrochemical potential of the dot. In effect, the ladder of electrochemical potential rises, and every time a level lies within the bias window, a Coulomb peak is observed (Fig. 2.2(a)). To observe the same Coulomb peaks, the other tunnel barrier defining gate would have to be raised (more positive) in voltage. Thus, when the two tunnel barriers are swept versus each other, one observes a series of parallel diagonals. The slope of the diagonal is a measure of the ratio of the capacitances of the tunnel barrier defining gates to the dot. This is the case for a single dot. In the case of a double dot, the diagonals are no longer parallel.

Figure 2.7: (a) Parallel diagonals representative of Coulomb oscillations as a function of the two tunnel barriers, indicative of a single dot regime. (b) Schematic stability diagram for two dots with intermediate tunnel coupling. Figure from [29]
(Fig. 2.7(a)) but instead exhibit a honey comb like structure (Fig. 2.7(b)) due to coupling between the two dots. Electron transport through double dots is discussed in detail by Wiel et al [29].

2.3 Quantum dots in disordered nanowires

The theory presented till now does not mention the effect of disorder. The quantum dots presented in the thesis are defined by gates in InAs/InP core shell nanowires. The mobility at low temperature of InAs nanowires varies between 1000-4000 cm$^2$/Vs [25, 2]. The low temperature mobility of bulk InAs is around $3\times10^5$ cm$^2$/Vs [10].

Figure 2.8: (a) A high resolution transmission electron microscope (HRTEM) image. The inset depicts the energy band diagram in the cross section of the wire. The scale bar is 10 nm. (b) A bright-field TEM of the core shell nanowire cross section. The dotted line indicates the interface between the layers and the surface of the shell. The scale bar is 5 nm [32]

Nanowires have a large surface to volume ratio. The surface of InAs has a large number of donor type surface states. Such a state is positively charged when empty. The electrons from these donors accumulate below the nanowire surface and cause the conduction band to bend downwards. When the number of surface states are large, the Fermi level lies above the conduction band minimum [13]. The surface accumulation
layer makes it possible to fabricate ohmic contacts, i.e., contacts without Schottky barriers to the nanowire. The conduction in the nanowire is mainly through the surface layer [28]. The reduced mobilities in the nanowire compared to the bulk may be due to enhanced scattering processes like ionized impurity and surface scattering [32]. Passivating the surface of InAs might reduce such effects. A 2-3 nm thin shell of Indium Phosphide (InP) is grown around the InAs wires to this effect. InP has a conduction band offset of 0.52 eV compared to InAs. Theoretical studies suggest a InP critical thickness of 2-3 nm for planar structures [31]. One expects that the lattice mismatch will be gradually relaxed radially outwards. The mobilities at low temperature for such core shell nanowires is around 10000 cm$^2$/Vs. A higher mobility implies a larger mean scattering length. Thus, with improved mobilities one expects less disorder in the conduction band compared to bare InAs nanowires.

Impurities and defects in the environment of the dot can cause local variations in the potential at the bottom of the well, depicted in Fig. 2.3. When the electron number is high, the device exhibits single dot behaviour. As the gate voltage is tuned, kicking out more electrons, at a certain point the dot can break up into a series of smaller dots due to the roughness of the conduction band. If the well depth of these smaller dots is similar then reaching the few electron single dot regime is not possible. One way of avoiding such a problem is to make the spacing between the gates defining the tunnel barriers small, comparable to the mean scattering length.

Figure 2.9: (a) Schematic depiction of the conduction band where a quantum dot is created with gate defined potential barriers. The Fermi level of the source and drain leads are shown. (b) Roughness of the conduction band causing a dot to break up into multiple dots as it is depleted.
Chapter 3

Fabrication

3.1 Nanowire growth

The nanowires used in this thesis are provided by Philips Research, Eindhoven, and are grown in a metal organic vapour phase epitaxy (MOVPE) reactor via the vapour-liquid-solid (VLS) mechanism. Catalytic Au particles are deposited from a colloidal solution on a substrate and placed in the reactor chamber. The temperature is around 420°C, with axial growth (VLS) as the dominant growth mechanism. The precursors for the nanowire core, Trimethyl Indium (In(CH$_3$)$_3$) and Arsine (AsH$_3$) are passed over the substrate in gaseous phase.

The precursor flux impinges directly on the gold particle, on the sidewalls of the nanowire, and on the substrate surface. Dissolving in the gold droplet, it forms an eutectic mixture, which supersaturates and crystallizes out at metal-semiconductor interface. It thus contributes to either the axial growth of the nanowire.

The wire growth is initially purely axial. The flux of precursor atoms on the substrate near the nanowire can reach the Au-nanowire interface by diffusion and contribute to axial growth, until the nanowire height exceeds the diffusion length of the adatoms [5]. At this point the lower part of the wire starts to grow radially leading to tapered nanowire growth. To grow the InP shell, the temperature is increased, and the precursor switched from Arsine to Phosphine (PH$_3$). At higher temperatures,
adatom diffusion is enhanced and radial shell growth dominates. The nanowires are typically 10 µm long and 60-100 nm thick. Figure 3.1 shows a SEM image of a nanowire batch thus grown.

### 3.2 Fabrication: Results and Discussion

Quantum dots have been created in nanowires using Schottky barriers in the contact [33] and heterojunctions. In our case, the quantum dot is defined by potential barriers due to metallic gates. Gate defined quantum dots offer the advantage of flexibility in terms of position and transparency of the tunnel barriers. The nanowires lie on top of a substrate that is degenerately p-doped Si with a thermally grown oxide layer on top. By applying a voltage to the substrate, referred to as the back gate, one can affect the overall electron density in the wire. The back gate is used in conjunction with the metal gates.

There are two approaches to fabricating such a device. One approach involves the fabrication of the gates (top and side gates) after nanowire deposition. The other (bottom gates) involves first the lithographic definition of the gates, and then
the nanowire deposition. A schematic depiction of the these configurations is presented in Fig. 3.2. Details of the fabrication procedure and recipe are discussed in Appendix A. In this chapter some issues of fabrication as well as consequences of gate geometry are presented and discussed.

![Schematic of gate orientations](image)

Figure 3.2: Schematic of the gate (grey) orientation w.r.t the nanowire (orange). The gates are isolated from the wire by a thin layer of oxide/dielectric (not shown in the figure)

### 3.2.1 Top gates

Depicted in **Fig** 3.2(a), the gates are designed to go over the nanowire, partially wrapping around it. The proximity and orientation allows for typically low operating gate voltages. Applying a negative voltage to a gate locally reduces the electron density, pushing up the conduction band. Increasing the negative gate voltage increases the height of the barrier above the Fermi level and no more electrons can flow. This pinch off voltage is typically within -2 V (**Fig. ??**). The gates are 35 nm wide, and around 35 nm apart (**Fig. 3.4**).

The gates comprise a layer of Aluminum and a layer of Gold. Aluminum has a grain size comparable to the width of the gates. Gold wets the grains and fills the gaps in between, preventing disconnected gates. In case a gate is not continuous, broken into smaller islands (**Fig. 3.3(a)**) around the nanowire, there are pieces of
Figure 3.3: Aluminum has a large grain size, comparable to the gate width. Employing just Al leads to disconnected gates as depicted in the schematic. A SEM image (b) of one such device shows the problems associated with grain size. (c) Schematic of a gate composed of Al & Au. (d) shows a SEM image of a device with such gates. The gates are narrow and continuous. The scale bar is 1 $\mu m$.

Metals that are essentially isolated from the electrical ground which can be charged and discharged. This would cause uncontrollable gating of the nanowire.

Contacts to the nanowires and the top (or side) gates are fabricated in two separate e-beam lithography (EBL) steps. The e-beam searches for a set of markers on the chip and the sample holder, which are used as a reference for writing a pattern. The search algorithm is not optimum and inter layer alignment errors can lead to pattern shifts of as much as 50 nm with respect to the original design. As a result, top gates might become partial top gates or accidental side gates Fig. 3.4.
Figure 3.4: (a) Top gates covering the nanowire without any patter shifts during EBL (b) A pattern shifted top gated device.

**Fig. 3.5** shows the typical pinch off curves from different wires using a top gate. The current pinches off around -1 V applied to a gate. The broad oscillations and shoulders in the curves may be due to universal conductance fluctuations, and are reproducible. The curves are also marked by spikes in current. Such fluctuations are random and change with every sweep. The dielectric plays a key role in the device performance, being responsible for gate isolation. Exposure to high energy electron beams during EBL, can lead to charging of the dielectric material [21], in this case the native oxide around the wire. Ionized atoms and other defects can act as charge traps. Due to direct contact between the gate and the native oxide around the wire, charges can hop from the gate into charge traps in the dielectric. Charges moving from one trap to another can change the electrostatic potential landscape. The net electrostatic effect is random fluctuations in conductivity or spikes, observed in the pinch off curves.

**Fig. 3.6(a)** shows the Coulomb peak oscillations as the gate potential of the left barrier ($V_L^G$) and right barrier ($V_R^G$) are swept versus each other. Blue represents the Coulomb blockade regions. Vertical shifts of portions of the plot can be attributed to charges hopping as discussed earlier. The data shown was taken over a period of 15 mins.
Figure 3.5: Typical top gate pinch off curves for the three different top gated nanowire devices. The bias voltage was 10 mV. The temperature was around 20 mK.

Suspecting defects and poor quality of the native oxide around the nanowire, different dielectrics were explored. A dielectric layer was deposited before lithographically defining the gates.

**Al₂O₃**

The wires were covered with a 20 nm thick layer of Al₂O₃ through atomic layer deposition (ALD). Fig. 3.6(b) shows pinch curves using the back gate for such a device. The trace does not show sharp fluctuations of conductivity. However, after top gate fabrication, the device behaviour changes drastically. The nanowire resistance decreases by a factor of ~2 (to around 10kΩ for a bias of 10 mV). The back gate voltage needed to pinch off current increased by a factor of 5. The top gates were unable to pinch off current for voltages upto -2 V. Exposure to high energy e-beam leads to ionization of the dielectric. The resultant charges screen the nanowire from the gates.

**SiO₂**

SiO₂ as a dielectric was deposited both by sputtering and evaporation. There was no observable improvement in the device stability for either of the two cases.

Charges hopping from the gate on to the defects in the dielectric were the main
Figure 3.6: (a) The figure shows Coulomb oscillations as one tunnel barrier is swept versus the other. Vertical shifts of portions of the plot are observed. This referred to as switching, occurs due to charges shifting from one defect in the dielectric to another, erratically changing the potential landscape. This measurement was taken over a period of 15 mins. (b) Shift in the electron density evident in the pinch off curves before and after top gate fabrication for devices with atomic layer deposition of Al₂O₃ as dielectric. Current was pinched off using the back gate, at a source-drain bias of 10 mV.

source of the observed instabilities. Physically and thus, electrically isolating the gates from the wire would reduce this problem.

3.2.2 Side gates

Side gates are designed to go right up to the nanowire but not make contact. The gates are 40 nm wide, and around 100 nm apart. As the gate and dielectric are physically separated, and the high quality thermally grown layer of SiO₂ has few defects, charge transfer from the gate to the dielectric is expected to be greatly reduced. Measurement data shows reduced switching (Fig 3.8(b)) compared to that from the top gated device (Fig 3.6(a)). The pinch off curves are smooth until erratic switches set in at higher gate voltages. The gates need higher voltages (∼ -10 V) in comparison to top and bottom configurations (Fig. 3.11). Fig. 3.8(b) shows data that was taken over an hour.
Alignment errors are an important issue in such a gate configuration. The gates need to be as close as possible to the nanowire, decreasing the gate voltage needed to pinch off. However due to pattern shifts, smaller this distance, greater are the chances of an accidental overlap of the gates and the nanowire.

A disadvantage of such distant gates is that the tunnel barriers formed are broad, as opposed to top or bottom gates. This combined with the disorder in the conduction
bands often results in intrinsic dots either under or close to the gate forming the tunnel barrier. It is difficult to tune the electrochemical potential of such dots. Fig. 3.2.2 shows the pinch off curve for a side gate. The inset shows a magnified part of the curve where Coulomb oscillations are visible. This is an indication of an unintentional quantum dot.

### 3.2.3 Bottom gates

Figure 3.10: Bottom gated device images taken with an SEM. (a) An array of patterned back gates (b) A typical bottom gated nanowire device. The scale bar is the same as (a).

A distinct change in the fabrication methodology compared to top and side gated
devices is that neither the dielectric nor the nanowire in the region where the dot is formed is exposed to high energy e-beam during EBL (accelerating voltage 100 kV). The fabrication steps involve first the lithographic definition of the gates, followed by selective dielectric deposition. After this step the nanowires are deposited and finally the underlying gates and the nanowire are contacted in one e-beam step. The dielectric is exposed to a lower energy e-beam during examination in an SEM (accelerating voltage 5 kV) but this does not cause any instabilities.

Figure 3.11: The figure show a comparison of pinch off curves using a top, side and bottom gate taken at a source-drain bias of 10 mV. From these curves one can gauge the typical operating voltage scales and stability of the measurement data for a given type of gate.

In conclusion, this goes a long way as far as the device response with respect to reproducibility and stability of data is concerned. Fig. 3.11 compares the pinch off curves from the three gate configurations. Top gates need lower operating voltages due to their proximity to the nanowire but defects in the dielectric often lead to unstable device response due to charges hopping from the gate on to the dielectric. Side gates in comparison are more stable, but need larger operating voltages and erratic fluctuations too occur beyond certain a certain voltage due to charges hopping between charge traps in the dielectric. However, since charges cannot hop from the gate on to the dielectric, switching is reduced. Bottom gates, on the other due to proximity to wire need voltages similar to the top gates, and do not exhibit the previously encountered switching in measurement data. This can be primarily attributed to the
absence of charge traps created in the dielectric on exposure to high energy e-beam, in region where the QD is defined. This comparison is depicted in Fig. 3.11. Bottom gates are the most stable of the three configurations discussed.
Chapter 4

Results and Discussion

In this chapter measurement data from the three gate configurations is presented. The basic mode of device operation is discussed. Then the results are discussed with respect to various themes such as stability, the few electron regime and the g-factor.

Quantum dots discussed here are defined by voltages applied to metallic gates in the vicinity of the wire. The gates are electrically isolated from the nanowire by either the native oxide on the wire or a layer of dielectric. Typically three gates are used to define and tune a quantum dot (Fig. 4.1). To this effect, one of the two outer gates (red) is driven to negative voltages till the current is nearly pinched off. Then voltage is applied on the other gate (red) till Coulomb oscillations are observed.

![Figure 4.1: A schematic depicting a nanowire orange), the leads (blue) and the three gates (red and black) typically used to define a quantum dot. The red gates define the confining potential barriers and the black gate, referred to as the plunger is used to tune the electrochemical potential levels of the dot.](image)

Due to capacitive coupling to the dot, changing the voltages on these gates also shifts the electrochemical potential of the dot, thereby kicking out electrons. However,
making the gate voltage negative makes the tunnel barriers higher, lowering the tunnel coupling of the dot to the leads. Beyond a point the current becomes too low to be distinguished from noise. For this purpose a middle gate (black), referred to as the plunger, is utilized. This gate couples to the dot without greatly affecting the tunnel coupling of the latter to the leads. The device lies on a degenerately p-doped Si substrate and a 285 nm thick layer of thermally grown SiO$_2$. A positive voltage applied to the back gate increases the electron density, raising the Fermi level. Presence of barriers due to charges on the surface or impurities produces barriers which shows up as a non-linear current versus voltage (I-V) profile. Raising the Fermi level over the level of these barriers can make the I-V curve linear. The devices are usually fabricated with five gates. The other gates are maintained at positive voltages to avoid barriers in that part of the nanowire.

4.1 Gated nanowire devices

In this section, brief details about the devices discussed later in this chapter, are presented.

Thenanowire used in the top gated device mentioned, has a diameter around 60 nm. The gates had a width of 30 nm, with the distance between two adjacent gates as 35 nm. The device was cooled down and electrically measured in a dilution refrigerator with a base temperature of 20 mK. The resistance of the device was around 100 kΩ at a bias of 10 mV. The pinch off curves using the top gates are shown in Fig. 4.2(a). The pinch off curves, taken at a bias of 10 mV, are relatively smooth devoid of frequent erratic jumps in current observed usually with other top gates (Fig. 3.5). This device was one of the more stable top gated devices.

The nanowire used in the side gated device discussed, has a diameter of around 60 nm. The side gates were 40 nm wide, and are around 100 nm apart. Unlike top gates, side gates do not touch the wire and are around 10 nm away from the wire. The device was cooled in a dip stick setup with a base temperature $\sim$ 1.6K. The device resistance at zero back gate voltage was $\sim$ 33 kΩ at a source-drain bias of
Figure 4.2: The figure shows pinch off curves from the devices with three difference gate configuration. The red curves correspond to the gates defining the tunnel barriers and the black is the middle gate used as a plunger.

10 mV. Due to the distance between the gates and the nanowire, larger operating voltages are required, evident in the pinch off curves, Fig. 4.2(b). The curves shown lack the frequent kinks exhibited by the typical top gate pinch off curves (Fig. 3.5). At voltages larger than -5 V, jumps in conductivity become quite frequent.

Data from two bottom gated devices is presented in this chapter. In both cases, the wire diameter is around 60 nm. In one case, the distance between the centre of two adjacent gates, the gate pitch is 100 nm and for the other, 65 nm. The former device was cooled in a dilution refrigerator with a base temperature of 20 mK. It had a resistance of 100 kΩ at zero back gate voltage. Pinch off curves for this device at a bias of 10 mV shown (Fig. 4.3) appear smooth and each gate pinches off the current within -1 V. The same curves taken at a bias of 1 mV show a lot of resonances probably due to universal conductance fluctuation (UCF). These resonances were time independent, reproducible with every gate voltage sweep. The second device was cooled in a similar refrigerator with a base temperature of 30 mK. The pinch off curves for this device at a bias of 10 mV, shown in Fig. 4.2(c) exhibits resonances due to UCF.
Figure 4.3: (a) Pinch off curves from a bottom gated device with a gate pitch of 100 nm, taken at a bias of 10 mV. The curves are smooth, devoid of erratic jumps in conductivity. (b) Some of the same curves retaken at a bias of 1 mV show pronounced resonances indicative of UCF.

4.2 Stability

The previous chapter discussed the general stability and reproducibility of measurement data for the three gate configurations, using pinch off curves to examine the same. Here the issue is discussed further using the charge stability diagram to highlight stability.

Keeping the voltages on the gates that define the tunnel barriers, constant the source-drain bias, $V_{SD}$ is swept versus the plunger gate voltage and a charge stability diagram is obtained (Fig. 4.4(a)). The Coulomb diamonds for the top gated device have been outlined, along with the first few excited states. The figure shows 9 electrons being kicked out of the dot as the plunger is tuned to more negative voltages.
Figure 4.4: The charge stability diagrams from a top, side and bottom gated device using the middle plunger gate.
The frequent fluctuations in the diamonds are quite evident. These vertical shifts in data occur due to charges hopping from one charge trap to another in the vicinity of the dot, leading to a change in the electrostatic gating of the dot, $\Delta V_G$. Switches of the order $\Delta V_G = 4$ are 20 mV are visible. They correspond to an energy change of 0.72 and 3.6 meV.

The Coulomb diamonds for a side gated device is shown in Fig. 4.4(b). The diamonds have been outlined as a guide, and a few excited state transitions marked in green. A noticeable change is the stability of the data compared to top gated devices. The frequent switches leading to small changes in the gating of the dot, are absent. The few switches observed in the data shown are all of the same order, $\Delta V_G \sim 24$ mV or 3.4 meV.

Fig. 4.4(c) shows the charge stability diagram for the bottom gated device with a gate pitch of 65 nm. The measurement data does not exhibit a single switch. It is stable and reproducible. The only change in the fabrication methodology is that the region where the QD is define is not exposed to e-beam. Thus charge hopping in the charge traps in the vicinity of the QD can be attributed as the cause of the previously witnessed instabilities.

4.3 Few electron regime

Fig. 4.4(a) shows the Coulomb diamonds for the top gated device. There is little variation in the addition energy, $E_{add} \sim 5$ meV. The current becomes too low before the diamond corresponding to the last electron is observed. From the excited state transitions (dotted lines), $\Delta E \sim 2$ meV. This gives the charging energy as, $E_C \sim 3$ meV. If one assumes parabolic confinement, then with $\hbar \omega = 2$meV, $d_{eff} \sim 114nm$. The distance between the tunnel barrier defining gates is around 130 nm. $\alpha$ factor is calculated to be $\sim 0.18$. Most top gated devices were plagued by instabilities such as the random jumps in the electrostatic gating to the dot. This was a major obstruction in tuning a dot to the few electron regime, while keeping the current resolvable.

As discussed in the previous chapter, as the side gates are far from the nanowire,
Figure 4.5: (a) Coulomb oscillations plotted as a function of the two tunnel barriers. Two sets of diagonals can be seen superimposed on each other - finely spaced diagonals representing a dot equally coupled capacitively to the tunnel barriers, and a broad widely spaced set, nearly parallel to the y-axis, representing an open small dot close to the tunnel barrier represented on the x-axis. (b) Schematic depiction of broad tunnel barriers which coupled with the roughness in the conduction band can lead to intrinsic dot. The nanowire (orange) and the tunnel barrier defining gates (red) are shown below the schematic.

compared to top gates, the tunnel barriers are broad. This combined with the roughness of the conduction band, leads to intrinsic barriers that can lead to multiple dots in series. Fig. 4.5(a) shows Coulomb oscillations as the two tunnel barriers are swept versus each other. The blue regions represent the Coulomb blockaded region. One set of finely spaced diagonals (dotted) seen corresponds to the dot between the two tunnel barriers. Given its equal capacitive coupling to the gates, it probably lies equidistant from the two gates. Another set of widely spaced broad diagonals (dashed) can also be observed, superimposed on the previous set, a sign of a double dot [29]. This can be attributed to an unintentional dot due to intrinsic barriers. The large spacing between the diagonals indicates that it is a small dot in comparison to the other dot. Due to a large asymmetry in its capacitive coupling to the gates, the dot probably lies under a gate or very close to it. These intrinsic dots were the main hindrance in trying to reach the few electron regime.
Figure 4.6: Coulomb diamonds obtained from the side gated device. (a) This figure is composed of two different sweeps, one encompassing a larger bias range as the addition energy increases. The dotted green line marked with an arrow indicate the excited state transitions. The data clearly reflects improved stability. (b) The tunnel barriers are lowered to enhance the current. $dI/dV_{SD}$ is plotted as a function of bias and gate voltage. The diamonds outlined in green corresponds to the one outlined in green in (a). One more diamond (blue) becomes visible, but the current could not be enhanced beyond what is visible. The Diamonds have been outlined as a guide to the eye. The excited state transitions have been marked with an arrow. The lines are thermally broadened with the temperature $\sim 1.6$ K or 500 $\mu$eV. $\left(4k_B T\right)$
Fig. 4.6 shows Coulomb diamonds from a side gated device, with differential conductance plotted as a function of bias and plunger gate voltage. The orbital energy, $\Delta E \sim 10$ meV. Assuming a spherical dot with parabolic confinement gives the $d_{eff} \sim 50$ nm. Fig. 4.4(b) shows a larger bias range sweep of the last two diamonds. The voltages on the tunnel barriers were tuned to enhance the current. $E_{add}$ is around 17 meV. The $\alpha$ factor is calculated to be $\sim 0.12$. Compared to top gates ($\alpha \sim 0.18$), the value is understandably lower as the distance of the gates from nanowire leads to lower capacitive coupling. Due to asymmetric confinement, one does not expect to see orbital degeneracy. As discussed earlier, an electron added to an empty shell will need to pay charging as well as orbital energy. The next electron would only need to pay the charging energy. This is seen as in the alternating sizes of the diamonds or addition energy $E_{add}$ seen, indicative of spin filling (Fig. ??sgd22) or Fig. 4.4(b)). Cottunneling leads to current visible within the diamonds in Fig. 4.4(b). All diamonds close and excited state transitions are visible. This supports the fact that this is a single dot. The last diamond, highlighted in blue does not close and seemingly goes on without kinks up to 50 mV source-drain bias. This could be the last electron, however given the low current, it is possible that the dot is still not empty and a few

Figure 4.7: (a) Coulomb oscillations show two set of diagonals superimposed on each other, a sign of two dots in series. (b) The device with 65 nm gate pitch exhibits single dot features.
more diamonds could be seen with the right tuning.  

**Fig.** 4.7 shows Coulomb oscillations as a function of the two tunnel barriers, for both the 100 and 65 nm gate pitch bottom gated devices. With a larger dot, due to roughness of the conduction band, the dot likely breaks up into multiple dots as it is depleted. In order to reach the few electron regime the roughness of the conduction band can pose a problem. This can be avoided by using gates of a smaller pitch, on the order of the mean scattering length.

![Coulomb diamonds](image)

Figure 4.8: The figure shows the Coulomb diamonds possibly corresponding to the last few electrons. The edges of the last diamond have been marked as a guide. At negative bias the dot shifts in position or changes shape, due to which its capacitive coupling to the source lead changes leading to a change in the slope of the edge. The excited state transition lines also follow this slope, remaining parallel.

**Fig.** 4.4(c) shows Coulomb diamonds from the bottom gated device. Alternating sizes of the diamonds can be seen. This is indication of spin filling. Co-tunneling current is seen within the diamonds. **Fig.** 4.8 shows Coulomb diamonds for the last two electrons. The last diamond, N = 1, gives a charging energy, $E_C$, of around 22 meV, and the excited state transition gives the orbital energy as $\Delta E = 15$ meV. The orbital energy for the diamond $N = 2$, is around 11 meV. The next diamond, $N = 0$, does not close and its edges go on without any observable kinks up to a source-drain
bias of 40 mV.

Assuming a spherical dot with parabolic confinement, as before, this gives a $d_{\text{eff}} \sim 50$ nm. The $\alpha$ factor is calculated to be around 0.15. One expects it to lie between that of partially wrap around top gates, and comparatively further side gates.

![Figure 4.9](image)

**Figure 4.9:** Coulomb oscillations as the two tunnel barriers are swept versus each other. (a) The figure shows the first two electrons are added to a single dot. After the addition of the second electron, the potential landscape changes such that the third electron is added to a double dot. The first two electrons in the figure correspond to the two parallel lines. After this a honey comb structure is observed, characteristic of a double dot [29] (b) This situation is schematically depicted with two wells, one lower than the other to which the first two electrons are added.

### 4.4 Zeeman splitting and g-factor

The g-factor for bulk InAs is $\sim -14.7$. As a result of the large g-factor (g-factor for GaAs is -0.44), Zeeman energy will have a large effect on the excited state spectrum. Fig. 4.10 shows magnified portions of a Coulomb diamond taken at a magnetic field of 0 and 2 T, perpendicular to the axis of the top gated nanowire. Splitting of the ground state and excited transition lines are visible and marked. From the splitting, $\Delta E_Z = 0.87$ meV for 2 T, the g-factor was calculated to be $\sim 7.5$.

The Zeeman splitting of the transition lines is examined under a magnetic field of
up to 5 T, applied in a direction perpendicular to the wire axis for a bottom gated device (Fig. 4.11). The rectangle outline indicates the area that is examined. Due to intentionally asymmetric barriers, transitions in one direction are more visible than the other. We observe a split in the ground state transition at negative bias for $B > 0$. The electron g-factor in bulk InAs is around -14.7. Due to confinement of the electron, the effective g-factor is expected to be higher [1, 9]. Theoretical predictions for a spherical InAs crystalline dot predicts that for a similar dot, the g-factor would still be negative [9]. Thus an electron added to an empty orbital will be a spin-up electron. This corresponds to the transition $GS(N) \rightarrow GS(N+1)$. Spin-up electrons have a lower energy than spin-down electrons due to the Zeeman splitting $\Delta E_Z = |g|\mu_B B$, where $\mu_B = 58$eV T$^{-1}$ is the Bohr magneton. Addition of a spin-up electron is energetically favoured. Addition of a spin-down electron will take the dot from $GS(N)$ to $ES(N+1)$, which is $\Delta E_Z$ higher in energy [27]. The $GS(N) \rightarrow ES(N+1)$ corresponds to a line that ends on the $N+1^{th}$ diamond, in this case $N = 1$. This transition is visible at the negative bias, ending on the $N = 1$ diamond.

Figure 4.10: Magnified section of the Coulomb diamonds at 0 and 2 T to show Zeeman splitting of transition lines. (a) The ground state and excited state transition lines have been marked with a line. (b) The splitting of the ground state (black line) and excited state (green line) transitions has been marked.
The Zeeman splitting $\Delta E_Z = |g|\mu_B B$ is indicated in the Fig. 4.11(b)-(f). The magnitude of splitting is $\sim 0.45, 0.94, 1.45, 1.94$ and $2.35$ meV for fields corresponding to $1 - 5$ T respectively. This gives the value of g-factor $7.8 - 8.2$. Averaging to remove noise leads to broadening of lines, hence an uncertainty in calculating the magnitude of the splitting. Other than the Zeeman split lines, a multitude of other lines parallel to the diamond edges are visible with a spacing that lies between $100$ and $250$ $\mu$eV. Such transition lines become stronger or weaker depending on the applied field. These lines also move, but gradually compared to the Zeeman split transitions, with changing magnetic field. The one dimensional nature of the nanowire leads to sharply peaked density of states. States in the dot moving into and out of resonance with these states lead to such transition lines [11, 15].
Figure 4.11: (a) Compared to the previous charge stability diagram (Fig. 4.8), the barriers have been tuned. Hence, the shift in the bottom gate voltage. The outline indicates the area that is examined under a magnetic field applied perpendicular to the wire axis. (b)-(f) Magnification of the diamond at fields 1 to 5 T. The Zeeman splitting is indicated. Apart from the split ground state transitions, a multitude of other lines are also visible, both of positive and negative conductance.
Chapter 5

Conclusions

From the results presented and discussed it can be concluded that:

- Top gates need low operating voltages, and are convenient to fabricate. Exposure of the dielectric to e-beam during e-beam lithography creates charge traps. Electrons hopping between these traps lead to erratic jumps in conductivity. These instabilities were a major obstacle in reaching the few electron regime.

- Using side gates instead, reduces the instabilities due to reduced hopping of charges from the gate into the dielectric. However, they need larger operating voltages (factor of 5). Side gates are susceptible to inter layer alignment errors during e-beam lithography and often partial top gates result.

- Side gates lead to broad tunnel barriers which combined with the roughness of the conduction band lead to small intrinsic dots under or close to the gate.

- Devices with bottom gates were fabricated in a different sequence of steps, the main change being that the region where the QD is defined is not exposed to high energy e-beam. This leads to a remarkable improvement of measurement data where switches occur rarely.

- A few electron dot tunable down to zero electrons was created using a bottom gate approach. Assuming parabolic confinement, the size of the dot was calculated to be around 50 nm.
• Zeeman splitting of the ground state and excited state transition lines was observed. The effective $g^*$-factor was calculated to be around 8. The value is expected to be higher than the g-factor of bulk InAs due to confinement and protrusion of the wavefunction into the InP shell. The g-factor of bulk InP is 1.2 [16].

• The bottom gate approach represents a reliable reproducible methodology for defining QDs in nanowires

5.1 Outlook

The bottom gate approach is a reliable method for fabricating nanowire devices where quantum dots can be defined and electrically measured. The data presented indicates stability and reproducibility. Thus, devices can be cooled down directly in dilution refrigerators. This skips the need to characterize the device in a quick cool down dip stick setup. Transferring a device from one setup to another can cause damage to the device. The next step would be to modulate the effective g-factor using the gates. By making the voltages on the gates that define the tunnel barriers more negative, one expects to squeeze the dot thereby changing $g^*$. For heterostructures, $g^*$ depends on the extent of the wave function in each material. Thus by using the plunger gate, it is may be possible to push the dot wave function into the InP shell, which changes the effective g-factor. Gate control over $g^*$-factor may be another way to coherently manipulate electron spins in a quantum dot.
Appendix A

A.1 Device fabrication

There are two approaches to device fabrication. The first involves nanowire deposition, followed by lithographic contacts to the wires, then the optional step of dielectric deposition and finally lithographically making gates aligned to the nanowire (top and side gate devices). The other comprises first the gate deposition (bottom gate devices), then the dielectric deposition, and finally in one step, the nanowire and the gates are lithographically contacted. The processing steps are discussed below and the details discussed later in the chapter.

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A.1.1 General

- **Substrate preparation**: A circular Si wafer cleaved into square bits is cleaned through the procedure outlined below:
• 2 min in Acetone in an ultrasonic bath
• 2 min in Ethanol in an ultrasonic bath
• 2 min in H₂O in an ultrasonic bath
• 2 min in HNO₃ in an ultrasonic bath
• 2 min in H₂O in an ultrasonic bath
• 2 min in Iso Propyl Alcohol (IPA) in an ultrasonic bath
• Blow dried with N₂

• **Markers**: The substrate is patterned with an array of bit markers. Each bit marker has a unique design which determines which row and column it lies in. Thus one can determine the position of a given nanowire with the aid of an adjacent bit marker. The bit markers are lithographically patterned with the same steps as contact fabrication but with 5 nm of Ti, and 60 nm of AuPd. These steps are discussed in greater detail later in the appendix.

• **Nanowire Deposition**: A simple method to deposit nanowires is the dry deposition technique. A strip of class 100 clean room paper, cut at sharp angles is used to lightly dab, first the mother chip containing the nanowire samples and then a Si/SiO₂ substrate. With this technique it is possible to control to some extent, the spread and regions where the nanowires are deposited. N₂ is blown onto the substrate to flatten the nanowires. One can find a reasonable number (∼ 10-15) of thin wires that are long, and fairly isolated.

• **Resist layers**

Two layers of resist are spun onto the substrate. The first, PMMA(17.5%)/MMA(8%) in Ethyl Lactate, is dripped onto the chip using a syringe, and spun for 60s at 3000 RPM. The measured thickness is ∼325 nm. The chip is then baked at 175°C for 10 min. The second layer, PMMA 950K, in 2% anisole, is dripped and spun at 3000 RPM for 60s. To minimize reaction between the two layers,
the delay between dripping and spinning should be kept to a minimum. This layer is baked at 175C for an hour. Baking reduces the sensitivity and hardens the resist which can minimize its mechanical stress and electron scattering into unexposed resist lines from adjacent exposed lines, resulting in minimal resist deformation during its development. For closely spaced structures, the undercut can overlap. In such a situation, only fine bridges of the upper resist layer remain which serve as a mask for metal deposition (Fig A.2). The thickness of this layer is \( \sim \) 90 nm. In this bilayer technique, the high molecular weight PMMA lies over the low molecular weight one. The low weight PMMA is more sensitive to electron exposure than the top layer, and the resist thus develops with an enhanced undercut. This increases ease of lift off.

- **Inspection**: The substrate is examined under an optical microscope. Though the typical nanowire diameter is less than the wavelength of light, it is visible under the microscope due to interference. Light is partially reflected at the resist surface and partially at the nanowire. Depending on the path difference between the light waves, they interfere constructively or destructively due to which the nanowire is visible. By focussing on the pre fabricated bit markers on the chip (65nm high) and then focussing a little closer to the substrate, one can select nanowires that are at the most 60 nm thick as they seem sharply defined, while thicker nanowires are blurred. Inspection can also be performed in an AFM or an SEM. Inspection under an SEM must be performed quickly, as it can lead to charging of the dielectric and the SiO\(_2\) layer. An AFM inspection is non destructive but can be time consuming.

- **Design & E-beam lithography (EBL)**: Images from the inspection are then inserted into a CAD file, and positioned by aligning the bit marker images with those on the design. Contacts or gates to the nanowires are designed, and the pattern is written on the resist layers using a high energy e-beam (accelerating voltage 100 KeV). The e-beam dose and spot size is varied depending on the size of the structures to be written, varying from 1100 \( \mu \)C/cm\(^2\) and spot size 20
nm for large structures, 1400 $\mu C/cm^2$ and spot size 2 nm for finer structures.

Figure A.1: A schematic illustrating the basic steps of resist exposure, metal deposition and lift off. The undercut in the lower resist layer, as depicted, helps in lift off

- **Developing & metallization**: The exposed resist is developed in a 1:3 solution mixture of Methyl Iso-Butyl Ketone (MIBK) and Iso Propyl Alcohol (IPA) for 60 s, followed by rinsing in IPA for 60 s. It is finally blow dried with $N_2$. To remove any organic residue, the substrate is exposed to oxygen plasma in a TEPLA 1000 chamber, at a power of 100 W for 15 s at a pressure of 1 mbar. The substrate is then etched in a buffered HF solution, to etch the oxide from the nanowires in the now exposed region in the resist layer. The chip is mounted in a metal evaporation chamber (TEMESCAL) and evacuated to $\sim 10^{-7}$ mbar. 10 nm of Ti, followed by 120 nm of Al is evaporated onto the chip at a rate of 1 A°/s.

- Lift off is done by placing the chip in hot acetone maintained at 55°C in a water bath, for an hour. This is followed by gently spraying cold acetone on the substrate and finally rinsing for 60 s in cold IPA.

## A.2 Chip carrier

The chip is diced with a diamond tipped cutter and glued to a chip holder using conductive silver paint. This allows for electrical contact to the degenerately p-doped Si substrate. Electrical contact to the contact pads on the chip is made by ultrasonic
bonding using Al/Si(1%) wires. The sample is ready to be loaded in the measurement setup.
Bibliography


